A SiGe 10-Gb/s Multi-Pattern Bit Error Rate Tester

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Abstract — **In this paper we present a monolithic IC that is capable of generating and evaluating multiple pseudo random bit sequences (PRBS) from DC to 10-Gb/s. This IC could be used as a low cost substitute for more expensive bit error rate test (BERT) systems.**

I. Introduction

Due to recent advances in high-speed communication systems, reliable testing of these systems has been an issue of concern. Pseudo random bit (PRB) sequences provide a convenient way of testing these high-speed components, and are mainly used for bit error rate and jitter measurements. The response of the device under test (DUT) for different pattern lengths often gives useful hints about the performance of the DUT. For example, a clock data recovery (CDR) unit will show higher jitter at longer pattern lengths due to the high run-length of ones and zeros in the pattern. A standard PRB sequence has a mark density ratio (defined as the average ratio of number of zeros to ones in a sequence) of 1/2. Modified PRB sequences that have mark densities other than 1/2 are used to characterize the dc behavior of the DUT. There have been monolithic bit error rate tester (BERT) IC's [1] developed in the past, which have one or two patterns. None of them have patterns longer than 2^{23}-1 or variable mark densities, which are essential for effective testing at speeds of multi-Gb/s.

In this paper we present a relatively low cost IC, developed in an advanced SiGe BiCMOS 0.25um process with an f_T of 80 GHz, which could act as a simple BERT. This IC is capable of generating PRB sequences of lengths 2^{31}-1, 2^{23}-1, 2^{15}-1, 2^{10}-1 & 2^{7}-1 with mark densities of 1/2, 1/4 & 1/8 for each of the patterns.

II. Design Description

Figure 1 shows a high-level schematic of the chip. It consists of a PRBS core, which can act as a generator or a detector depending on the mode selected, a mark density generator that alters the pattern to give the required mark density and an error detector. The pattern length and the mark density of the output pattern are controlled by the use of static external signals (s0, s1, s2, m0, m1). Another static signal enc/dec is used to switch the core between generator and detector modes. The outputs include the required pattern, error signal (monitored, when used in detector mode), a differential clock output and a divided clock output (for triggering purposes). All the high-speed inputs and outputs are 50 ohm terminated with CML levels.

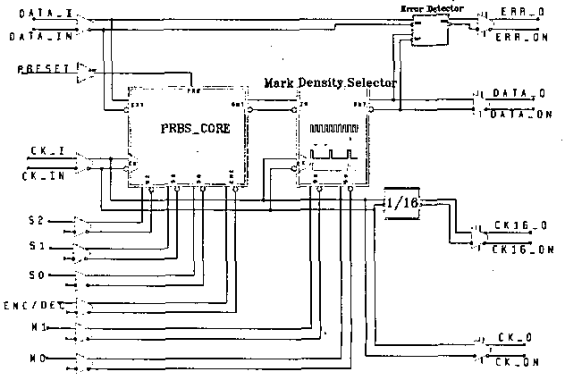

Figure 1. Top Schematic of the BERT IC.

The chip works with a nominal supply of –3.3V. The low supply voltage poses a limitation on the number of levels of BJTs that can be stacked. The following figure shows a typical latch used in the chip. All other basic logic gates (ands, ors & xors) are derived from simple modifications of this basic latch. The delays through these logic gates and the clock→Q delay of the flip-flops determine the maximum frequency of operation.

Figure 2. Typical CML Latch used in the BERT IC.

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A. PRBS Core

The primary function of the core is to generate or analyze PRB sequences. The sequence is chosen depending on the sequence select signals. A high-level block diagram of the core is shown in Figure 3. The first mux in Figure 3 is used to select a particular sequence and the second mux is used to switch the core between generator and detector modes. In a typical single pattern PRBS generator only one feedback loop with one xor is present, whereas in our case five possible feedback loops are present with only one loop closed at a time, depending on the sequence select signals applied to the core. In the actual design this 5-1 mux is implemented using four 2-1 'mux's. Due to timing constraints, the signal is allowed only one gate delay (e.g. a mux) before it should be retimed again, thereby requiring that the output of every mux/xor/and be retimed. While doing this, care should be taken that the number of delays in each loop still remains the same. This is important because there are fixed combinations of taps that generate PRB sequences and changing the number of delays would disturb those tap combinations.

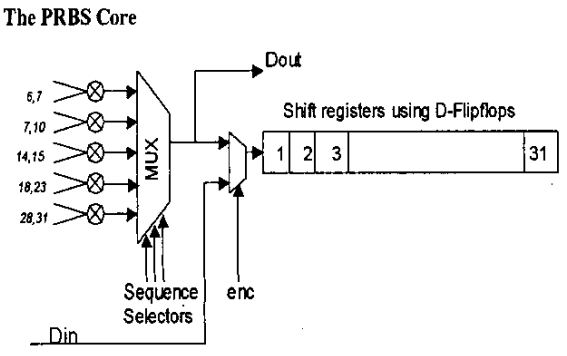

Figure 3. High-level diagram of the PRBS core. The numbers shown are the taps from the shift register. Its inputs are the three sequence selectors (s0, s1, s2), the input stream Din (needed only in detector mode) and the clock. Its output is the Dout.

When the core works as a generator one of the feedback loops is closed and the 'Dout' that comes out of the core would be a PRB sequence of the required length. When the core runs in the detector mode, the loop is broken and the error detection is based on the principle by Westcott [2]. At the location where the loop is broken, the incoming stream is compared with the bit stream regenerated in the core. This is how error detection is done usually in a PRBS detector [1]. One problem associated with this approach is that a single error in the incoming stream causes multiple error pulses in the output. This problem is overcome by closing the loop once the core is synchronized with the external data coming in. The core sync can be observed externally by monitoring the 'ERR' signal. A static 'ERR' signal indicates that the core is in sync with the external data stream. Once sync has been observed in the core, the loop should be closed, by making the 'enc/dec' signal high. In this mode the IC behaves as an error detector.

B. Mark Density Generator

The output of the core 'Dout' along with the mark density select signals are fed to the mark density generator. The variable mark density generator is built on the simple idea that 'and'ing a PR stream with a delayed version of itself would produce a stream with an average mark ratio of ¼.

In a regular PR stream, Probability (0) = Prob (1) = 1/2.

When two adjacent bits are 'and'ed, a 1 appears at the output only if both the bits are 1. So, Prob(1) = (1/2)*(1/2) = ¼. (This probability calculation assumes that the sequence is uncorrelated with a delayed version of itself, which is true in the case of PRB sequences.) This idea can be used to generate sequences with mark ratio's of 1/8, 1/16... and so on. In this chip we generate mark ratios of 1/4 and 1/8. The actual circuit used is shown in Figure 4. The additional delays are added to match the delays at all stages of 'and'ing and 'mux'ing. In a low frequency situation where the propagation delays through the logic gates are small compared to the time periods, the retimers after the 'and' and 'mux' would not be necessary.

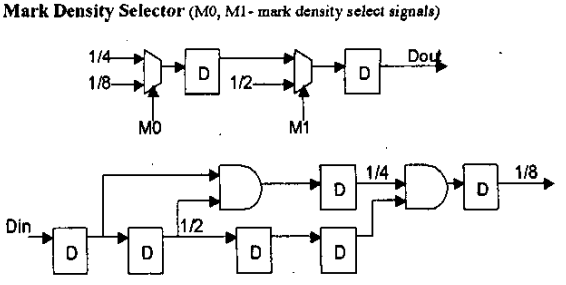

Figure 4. Schematic of the mark density generator. Its inputs are the two select signals M0, M1 and the output of the core. Its output is the pattern output, which also goes into the Error detector circuit.

C. Error Detector

The error detector compares the output of the mark density selector 'Dout' with the bit stream 'Din' that

goes into the core. The delays of these two streams have to be matched before any comparison is made. This delay turns out to be 3, which is in the mark density selector. The error detector generates a pulse whenever there is an error in the incoming stream. This error pulse can be fed into an external microwave counter to count the exact bit error rate of the incoming test pattern.

III. Typical Test Setup

In a typical setup, we have a Generator, a Device Under Test (DUT) and an Error Detector connected as shown in Figure 5. The ENC_G signal of the generator is always held high. The ENC_D signal of the Error detector is held low during the initial training, where its internal generator synchronizes with the input it receives from the DUT. Synchronization is achieved when there are no errors for 32 consecutive clock cycles.

After the Sync, the ENC_D of the error detector should be turned low to enable it to count errors. Also, during synchronization, the mark select signals M0 & M1 should be set low, both at the generator and the detector.

Figures 6 and 7 show typical output patterns seen during simulations. In Figure 6, where mark density ratio is ½, the number of zeros and ones are approximately equal. Whereas, when mark density is 1/8 (Fig 7) the pattern has 8 '0's for every '1' on an average.

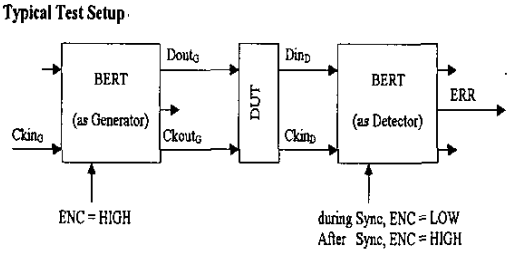

Figure 5. This shows a typical test setup, where the BERT is used as a generator and an error detector. The detector needs to be synchronized to the incoming Din_D, before errors can be measured.

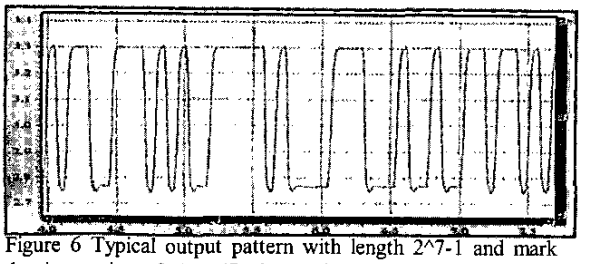

Figure 6 Typical output pattern with length 2^7-1 and mark density ratio of ½. (Scale: time: 500ps/div, voltage: 100mV/div)

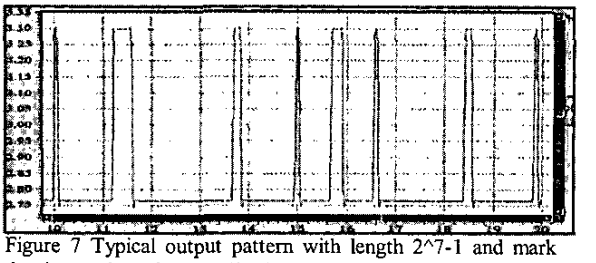

Figure 7 Typical output pattern with length 2^7-1 and mark density ratio of 1/8. (Scale: time: 500ps/div, voltage: 100mV/div)

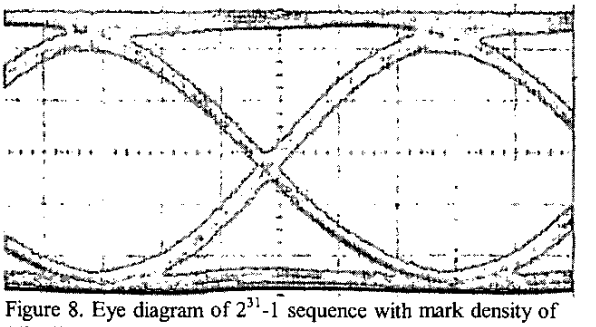

Figure 8. Eye diagram of 2^{31}-1 sequence with mark density of 1/8. (Scale: time: 16.8ps/div, voltage: 100mV/div). Notice how the bottom line is much thicker than the top line, which shows there are more zeros than ones in the pattern.

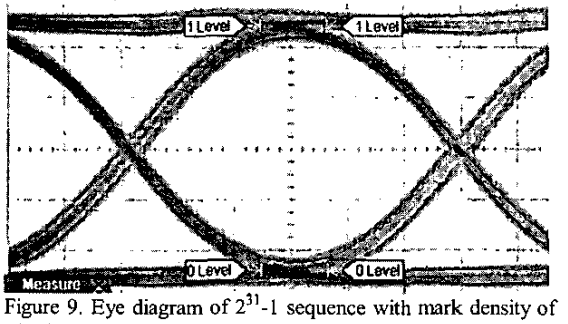

Figure 9. Eye diagram of 2^{31}-1 sequence with mark density of 1/2. (Scale: time: 17.2ps/div, voltage: 100mV/div)

IV. Measurement Results

The IC was tested on a custom made printed circuit board. All five possible pattern lengths have been verified by observing the separation of the spectral peaks. This data matched with the theoretical calculations (Separation = Data-rate/(Pattern-length)). Mark densities of all the possible patterns are also tested by measuring their DC levels. These tests confirm the operation of the BERT as a pattern generator. Once the BERT is tested as a generator it can be used as a pattern generator to test the BERT in its detector mode. Note that this needs 2 different BERT IC's as the BERT can't be in both generator and detector modes at the same time. The test setup for this test is similar to the one in Figure 5, but without a DUT. The output of the generator is connected directly to the input of the Detector. The ERR output of the Detector was found to be zero after the initial training for all the different patterns.

Figures 8 and 9 show different measurements obtained from the IC. As shown in the figures the eye diagrams showed the difference between different mark density ratios. Table I shows the key performance figures of the BERT IC.

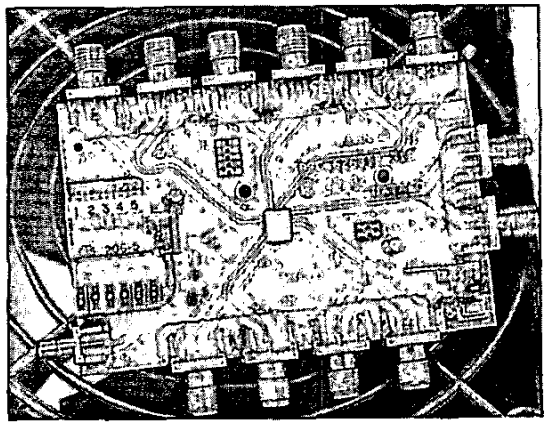

Figure 10. The PCB board with the test IC mounted in the center

V. Process Description

This SiGe process consists of a base of 0.25um CMOS with Bipolar modules and mixed signal options. The Ft of the HBT device is 80GHz, with and Fmax of 100GHz [3]. The metal system has 4 levels with high planarity and stackable vias. Metal-Insulator-Metal (MIM) capacitors provide very high quality elements for tuned circuits and decoupling. Polysilicon resistors are available in several resistance ranges; these have low parasitic capacitance because they are laid down on the field oxide.

VI. Conclusions & Future Work

This IC is redesigned on a faster SiGe BiCMOS process with an f_T of 120 GHz. The redesigned IC consumes about 25% less power and is expected to have a better eye at 10GHz. A companion chip, which generates 4 well-spaced[1] PRB patterns from a single PRB pattern, is also developed. This chip in conjunction with the BERT chip could be used to test a wide variety of high-speed multiplexers and demultiplexers.

TABLE I
SUMMARY OF BERT PERFORMANCE

Max generator speed	15 Gb/s
Max detector speed	13 Gb/s
Nominal Supply	-3.3V
Power Dis @3.3V	2.3W
Chip Size	2*1 mm^2
Output Swing	500mV (Diff)
Output Jitter	7.7 ps p-p @ 10Gb/s
Mark densities	1/2, 1/4, 1/8
Sequence lengths	2^{31}-1, 2^{23}-1, 2^{15}-1, 2^{10}-1 & 2^{7}-1

Acknowledgement

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References

[1] O. Kromat et al "A 10 Gb/s silicon bipolar IC for PRBS testing." *In Int. Solid-state Circuits Conf. (ISSCC) 1996, Dig. Tech. Papers*, pp. 206-207

[2] R. Westcott, "Testing digital data transmission systems," U. K. Patent 1 281 390, 1972.

[3] D. Knoll, B. Heinemann, K.E. Ehwald, H. Rücker, B. Tillack, W. Winkler, and P. Schley, "BiCMOS Integration of SiGe:C Heterojunction Bipolar Transistors," *2002 IEEE Bipolar/Bicmos Circuits and Technology Meeting Proceedings*, pp. 162-166.

[1] The 4 patterns are not symmetrically (1/4 *Pattern Length) spaced. However, the spacing is sufficient to make the 4 outputs uncorrelated for all practical purposes.